1. Claims 1-7 are presented for examination.

2. Claims 8-45 withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected inventions, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 07/16/07.

3. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Nunomura (6,871,274).

4. Claims 6,7. are rejected under 35 U.S.C. 103(a) as being unpatentable over Nunomura (6,871,274) in view of Rim (6,202,143).

5. Claim 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Trembly et al. (5,925,123).

6. The rejections are maintained and incorporated by reference the last Office action on 09/24/07.

7. The response filed on 12/27/07 has been fully considered but is not persuasive.

8. In the remarks, applicant argued that :

a) Applicants note that all recited claims were previously examined, in rejections dated 6/26/06 and 12/20/06. Such history of previous examination appears to infer that the examination is not seriously burdensome, and that therefore the required "serious burden" is not present.

b) "If the search and examination of all the claims in an application can be made without serious burden, the examiner must examine them on the merits, even though they include claims to independent or distinct inventions" (MPEP § 803, emphasis added);

c) For these reasons, Applicants respectfully assert that the classifications of the alleged Group I inventions are incorrect, and respectfully solicit correction of the classification;

d) Group I recites "executing on said processor said second machine language instruction." Thus, an apparatus for implementing the method of Group I must have a processor capable of executing machine language instructions, in contrast to the rejection's allegation. Further, Group III recites all the limitation of independent Claim 1 (Group I).

e) Nunomura teaches that the relied upon teaching is not "a machine language instruction" as claimed by Claim 1. Nunomura's "compressed

f) Nunomura teaches that the "compressed instruction code" is "unrecognizable as an instruction code" (column 7 lines 30-37).

g) Nunomora did not teach or suggest the limitation of "modifying said instruction segment" as recited by Claim 1;

h) Figure 4 shows a four-bit "index" mapping into a 24 bit op code. Applicants respectfully assert that a code segment "longer in bit length than the first code" as taught by Nunomura, cannot be the recited "instruction segment" that is part of the recited first machine language instruction;

i) Nunomura fails to teach or suggest the limitation of "substitut(ing) a bit pattern of a subset of said instruction segment" as recited by Claim 2. In contrast, Nunomura teaches "substituting" more bits than an instruction segment contains. In this manner, Nunomura actually teaches away: from the recited limitation of substituting a subset of bits of an instruction segment, as recited by Claim 2;

j) 702 (Figure 7). Further, Tremblay is absolutely and completely silent as to forming a "second machine language instruction" from a first machine language instruction" as recited by Claim 1;

k) Rim teaches multiple program memories for storing multiple sizes of instruction words, and that the multiple program memories "preferably have different (bus) widths" (Abstract). In contrast, Nunomura teaches a single memory with a single bus size. Applicants respectfully assert that one of ordinary skill in the art would not be motivated to combine these references in the manner suggested because of the complexity of Rim in contrast to the relative simplicity of Nunomura;

l) there is no teaching in the prior art as to the desirability of modifying Nunomura to accept VLIW instructions;

m) Nunomura teaches a method of storing instructions in a compressed format. In contrast, Rim teaches a method of expanding a complete uncompressed instruction with meaningless filler (a "NOP" or no operation instruction) to fill a wide bus. Applicants respectfully assert that, in consideration of the whole of the teachings of Nunomura and Rim, one of ordinary skill in the art would not be motivated to modify a decompression

process with a process that places meaningless filler into an instruction word. Moreover, Nunomura has no need for the filler methods of Rim, as Nunomura has a single bus and a single bus width;

n) as recited by Claim 6. Applicants are unclear as to what format a compressed instruction code might have under the modification proposed by the rejection, but respectfully assert that such a compressed instruction code would not be a very long instruction, word as specifically recited by Claim 6;

o) applicants understand that it is the intention of Nunomura to reduce the size of such compressed instruction codes. Hence, Nunomura leads away from the recited fetching VLIW machine language instructions as recited by Claim 6.

As to a) Number of references used is irrelevant to restriction requirement. The fact that a single reference was used , it did not necessarily mean that it did not present serious burden to examiner. In fact, it presented serious burden to examiner as shown in restriction requirement (e.g. see pages 4-5) set forth in office action on 06/12/07. Therefore, it will not be repeated herein.

As to b), "IF..." (MPEP § 803, emphasis added).

As to c), applicant failed to point out correct classifications. Nevertheless, examiner holds that the classifications the alleged Group I-VI invention were incorrect as set forth in the restriction requirement on 06/12/07.

As to d), an apparatus for implementing a method of Group I does not necessarily have a processor capable of executing machine language instructions.

As to e), Nunomura taught :

1) fetching a first machine language instruction (tran instruction) comprising an instruction segment [TRANS 1100 0010 0001 0010] (see the dispatched instruction from the prefetch unit in co1.5, lines 50-54);

2) responsive, or recognizing, or based on, to a trigger pattern [index] in said first machine language instruction (see machine language in fig.4), modifying said instruction segment to form a second machine language instruction (see 1001 1111 1100 0000 0000 0010 0001 0010 in fig.4, col.6, lines 27-50).

If the machine language instruction (see 0' and 1' in fig.4) is not a machine language , can applicant show what he thinks as a machine language instruction ?

As to f), applicant is taking a portion out of context. The cited portion was for exception cases (see col.7, lines 30-37).

As to g), Nunomura taught a segment of the "compressed instruction code" is replaced by a second code "longer in bit length than the first code" (column 2 lines 18-19). Nunomora did teach the "modifying said instruction segment"

As to h), Nunomura taught a segment of the "compressed instruction code" is replaced by a second code "longer in bit length than the first code" (column 2 lines 18-19). Therefore, Nunomura taught "instruction segment" that was part of the first machine language instruction by replacement.

As to i), Nunomura teaches "substituting" more bits than an instruction segment contains (column 2 lines 18-19). Nunomura did teach the recited limitation of substituting a subset of bits of an instruction segment, as recited by Claim 2.

As to j), Trembly taught forming a "second machine language instruction" from a first machine language instruction" as recited by the claim (see fig.7 for opcode for instruction segment, co1.27, lines 40-54 opcode, see the trigger pattern [mode] in the first machine language instruction, modifying the instruction segment to form a second machine language instruction [microcode]).

As to k), multiple program memories encompassed single program memory. And, the difference between multiple program memories and a single program memory is not complex, and it's easily recognizable by one of ordinary skill in the art.

As to l), examiner holds that VLIW instruction had been known in the art. Thus, Nunomura could be modified in view of Rim to "recognize ... specific instruction type with corresponding width of the Rim's VLIW," the proposed combination would be able to execute such VLIW instructions. Therefore, examiner asserts that one of ordinary skill in the art would be motivated to modify Nunomura in view of Rim, in the manner proposed by the rejection, to "recognize" VLIW instructions based on the known VLIW capability to execute such instructions.

As to m), one of ordinary skill in the art would be motivated to modify a decompression process with a process that places meaningful filler, such as NOP in the practical application of expansion as taught by Rim, into an instruction word.

As to n), a compressed instruction code under the modification proposed by the rejection would be a very long instruction, word as specifically recited by Claim 6 because of the need for compression.

As to o), reducing the size of compressed instruction codes is s applicable in VLIW.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

/Daniel Pan/
Primary Examiner, Art Unit 2183